III. REMARKS

Claims 12-18 and 20 are pending in this application. Applicants do not acquiesce in the correctness of the rejections and reserve the right to present specific arguments regarding any rejected claims not specifically addressed. Further, Applicant reserves the right to pursue the full scope of the subject matter of the original claims in a subsequent patent application that claims priority to the instant application. Reconsideration in view of the above amendments and the following remarks is respectfully requested.

The Examiner has made this Office Action final although the examiner has introduced a new ground of rejection that is neither necessitated by applicant's amendment of the claims, nor based on information submitted in an information disclosure statement. Specifically, the Examiner has introduced a new reference Yoo et al. (US 6,168,984). This is improper and Applicants request that the finality of this rejection be withdrawn.

In the Office Action, claims 12-20 are rejected under 35 USC §112, second paragraph, as allegedly being indefinite. Specifically, the Office interprets "probable" in the definition of "damaging temperature" as "establishing a probability" and asserts that "the specification does not establish a probability of damage at the silicidation temperature[.]" (Office Action at page 2). Applicants respectfully disagree because the Office applies an apparently non-applicable interpretation of the term "probable". The Office is improperly importing this limitation into the claims. This is not permissible. *Altiris Inc. v. Symantec Corp.*, 318 F.3d 1363, 1371, 65 USPQ2d 1865, 1869-70 (Fed. Cir. 2003). The claim language states wherein the silicide section has a silicidation temperature less than a damaging temperature of the plurality of BEOL layers. This language on its face is clear to the skilled artisan as silicidation temperature, damaging

temperature and BEOL layers are all clear to a person of ordinary skill in the art. Applicant has provided an invention that allows for passive resistor to be processed without high temperature anneals that would damage other BEOL wiring structures [paragraph 0004]. Either the BEOL wiring layers are damaged or they or not, there is nothing indefinite in this language. In view of the foregoing, Applicants respectfully request withdrawal of the rejection under 35 USC §112, second paragraph.

In the Office Action, claims 12, 18 and 20 are rejected under 35 U.S.C. §103(a) as being anticipated by Yoo et al. (US 6,168,984), hereinafter "Yoo", and claims 13-17 are rejected under 35 U.S.C. §103(a) as being unpatentable over Yoo in view Wolf, *Silicon Processing for the VLSI Era*, 1990, Volume II, pp 146, 176, 193 hereinafter "Wolf." Applicants respectfully submit that the claimed subject matter is allowable for the reasons stated below.

With respect to anticipation rejection of claims 12, 18 and 20, the Examiner asserts that Yoo discloses a silicide resistor formed of a poly-silicon layer and a tungsten silicide layer. The Examiner asserts that the structure referenced in the Figure 13 of Yoo has an inherent resistance and thus considered a resistor in one of a plurality of BEOL layers (formed from an interlayer dielectric over FEOL layers 1-17, layer 31 is a second BEOL layer, thus 27 and 31 are a plurality), the silicide section having a silicidation temperature less than a damaging temperature of the plurality of BEOL layers. This argument ignores the teaching of Yoo. The structure referred to in Yoo adds an insulator layer 31 to allow for a capacitor structure to be constructed thereon. Thus, the characterization that Yoo teaches a silicide resistor is faulty. The polysilicon layer and tungsten silicide layer of Yoo is defined at a polycide bitline structure. A bitline is not

a resistor. Therefore, Yoo does not teach every element of the instant invention and the anticipation rejection must be removed.

With respect to claims 13-17 Wolf is cited for teaching group VII silicides. Such disclosures of the silicides substituted into the structure of Yoo would not produce Applicants invention. There would not be a silicide resistor as claimed but a bitline for use in a DRAM semiconductor device. In addition, both Wolf references only disclose using the silicide materials for interconnect applications, not for a resistor application as claimed in the current invention. Therefore a combination of the references does not provide a silicide resistor.

The dependent claims are believed allowable for the same reasons stated above, as well as for their own additional features.

Applicants respectfully submit that the application is in condition for allowance. Should the Examiner believe that anything further is necessary to place the application in better condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number listed below.

Respectfully submitted,

/Spencer K. Warnick/

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